DATA SHEET

74LVC16244A; 74LVCH16244A
16-bit buffer/line driver; 5 V input/output tolerant (3-state)

Product specification
Supersedes data of 2002 Oct 30

2003 Jan 30

Philips Semiconductors

PHILIPS

FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold (74LVCH16244A only).
- Complies with JEDEC standard no. 8-1A
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.

DESCRIPTION

The 74LVC(H)16244A is a high-performance, low power, low voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 Volt. These features allow the use of these devices as a mixed 3.3 and 5 V environment.

The 74LVC(H)16244A is a 16-bit non-inverting buffer/line driver with 3-state outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high-impedance OFF-state.

The 74LVC(H)16244A is identical to the 74LVC16240A but has non-inverting outputs.

The 74LVCH16244A bushold data inputs eliminates the need for external pull-up resistors to hold unused inputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA_n to nY_n	C_L = 50 pF; V_{CC} = 3.3 V	3.0	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	V_I = GND to V_{CC}; note 1	25	pF

Note

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz;

   f_o = output frequency in MHz;

   C_L = output load capacitance in pF;

   V_{CC} = supply voltage in Volts;

   N = total switching outputs;

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC16244ADL	–40 to +85 °C	48	SSOP48	plastic	SOT370-1
74LVCH16244ADL	–40 to +85 °C	48	SSOP48	plastic	SOT370-1
74LVC16244ADGG	–40 to +85 °C	48	TSSOP48	plastic	SOT362-1
74LVCH16244ADGG	–40 to +85 °C	48	TSSOP48	plastic	SOT362-1
74LVC16244AEV	–40 to +85 °C	56	VFBGA56	plastic	SOT702-1
74LVCH16244AEV	–40 to +85 °C	56	VFBGA56	plastic	SOT702-1

FUNCTION TABLE

See note 1.

INPUT		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	L
L	H	H
H	X	Z

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don’t care;
   Z = high-impedance OFF-state.

PINNING

SYMBOL	PINS	BALLS	DESCRIPTION
$1\overline{OE}$	1	A1	output enable input (active LOW)
n.c.	–	A2, A3, A4, A5, E3, E4, F3, F4, K2, K3, K4, K5	not connected
$1Y_0$	2	B2	data output
$1Y_1$	3	B1	data output
GND	4, 10, 15, 21, 28, 34, 39, 45	B3, B4, D3, D4, G3, G4, J3, J4	ground (0 V)
$1Y_2$	5	C2	data output
$1Y_3$	6	C1	data output
V_{CC}	7, 18, 31, 42	C3, H3, C4, H4	supply voltage
$2Y_0$	8	D2	data output
$2Y_1$	9	D1	data output
$2Y_2$	11	E2	data output
$2Y_3$	12	E1	data output
$3Y_0$	13	F1	data output
$3Y_1$	14	F2	data output
$3Y_2$	16	G1	data output
$3Y_3$	17	G2	data output
$4Y_0$	19	H1	data output
$4Y_1$	20	H2	data output
$4Y_2$	22	J1	data output
$4Y_3$	23	J2	data output
$4\overline{OE}$	24	K1	output enable input (active LOW)
$3\overline{OE}$	25	K6	output enable input (active LOW)
$4A_3$	26	J5	data input
$4A_2$	27	J6	data input
$4A_1$	29	H5	data input
$4A_0$	30	H6	data input
$3A_3$	32	G5	data input
$3A_2$	33	G6	data input
$3A_1$	35	F5	data input
$3A_0$	36	F6	data input
$2A_3$	37	D6	data input
$2A_2$	38	E5	data input
$2A_1$	40	D6	data input
$2A_0$	41	D5	data input
$1A_3$	43	C6	data input
$1A_2$	44	C5	data input
$1A_1$	46	B6	data input
$1A_0$	47	B5	data input
$2\overline{OE}$	48	A6	output enable input (active LOW)

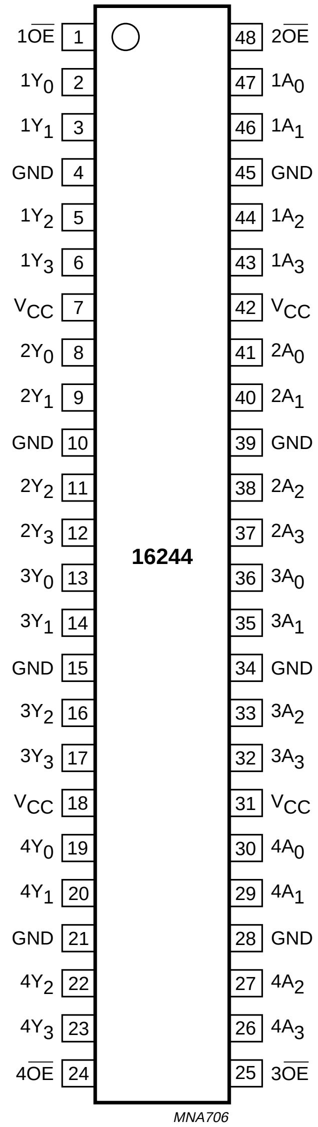


Fig.1 Pin configuration SSOP/TSSOP48.

	1	2	3	4	5	6
A	$1\overline{OE}$					$2\overline{OE}$
B	$1Y_1$	$1Y_0$	GND	GND	$1A_0$	$1A_1$
C	$1Y_3$	$1Y_2$	V_{CC}	V_{CC}	$1A_2$	$1A_3$
D	$2Y_1$	$2Y_0$	GND	GND	$2A_0$	$2A_1$
E	$2Y_3$	$2Y_2$			$2A_2$	$2A_3$
F	$3Y_0$	$3Y_1$			$3A_1$	$3A_0$
G	$3Y_2$	$3Y_3$	GND	GND	$3A_3$	$3A_2$
H	$4Y_0$	$4Y_1$	V_{CC}	V_{CC}	$4A_1$	$4A_0$
J	$4Y_2$	$4Y_3$	GND	GND	$4A_3$	$4A_2$
K	$4\overline{OE}$					$3\overline{OE}$

MNA702

Fig.2 Pin configuration VFBGA56.

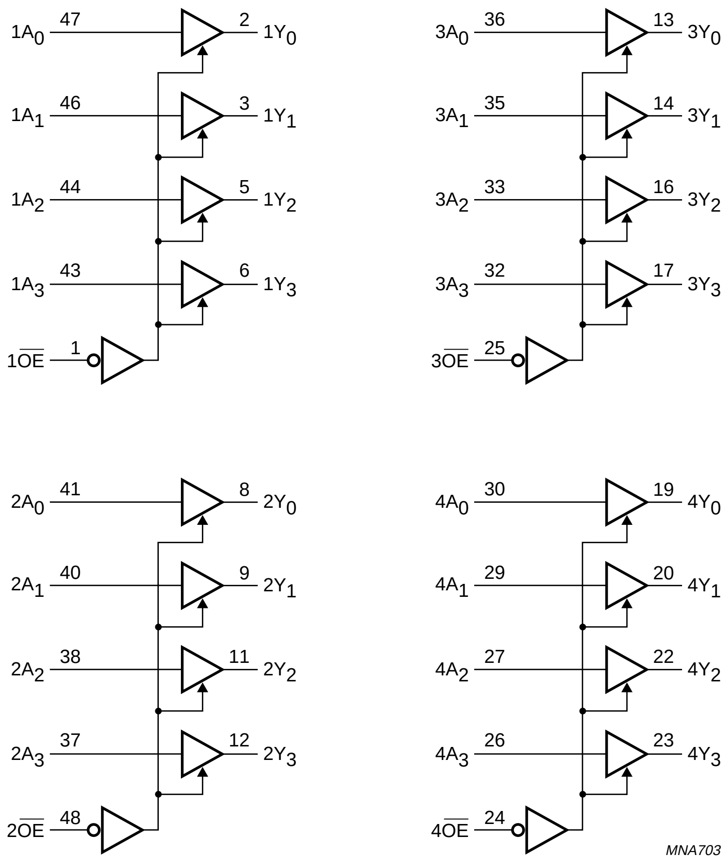


Fig.3 Logic symbol.

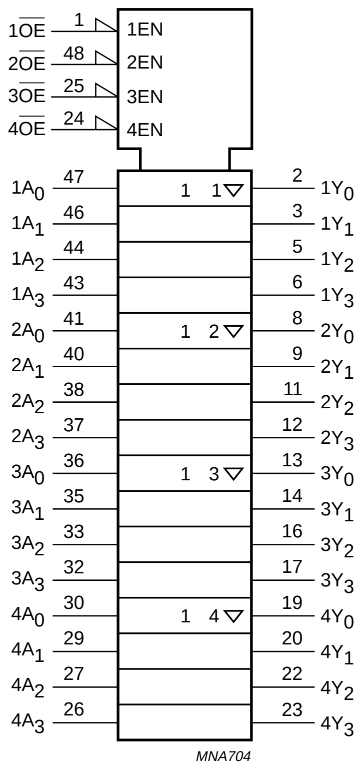


Fig.4 Logic symbol (IEEE/IEC).

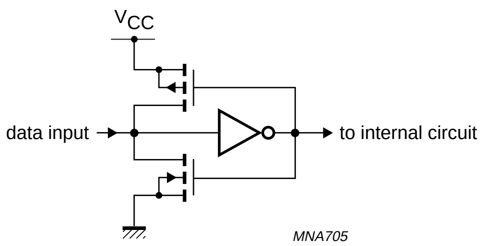


Fig.5 Bushold circuit.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low voltage applications	1.2	3.6	V
V_I	input voltage		0	5.5	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
		output 3-state	0	5.5	V
T_{amb}	operating ambient temperature	in free air	–40	+85	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$	–	–50	mA
V_I	input voltage	note 1	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	output voltage	output HIGH or LOW state; note 1	–0.5	V_{CC} + 0.5	V
		output 3-state; note 1	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation;				
	SSOP and TSSOP package	temperature range from –40 to +85 °C; note 2	–	500	mW
	VFBGA package	temperature range from –40 to +85 °C; note 3	–	1000	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 60 °C the value of P_D derates linearly with 5.5 mW/K.
3. Above 70 °C the value of P_D derates linearly with 1.8 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.[1]	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = –40 to +85 °C							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –12 mA	2.7	V_{CC} – 0.5	–	–	V
		I_O = –100 μA	3.0	V_{CC} – 0.2	V_{CC}	–	V
		I_O = –18 mA	3.0	V_{CC} – 0.6	–	–	V
		I_O = –24 mA	3.0	V_{CC} – 0.8	–	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 12 mA	2.7	–	–	0.40	V
		I_O = 100 μA	3.0	–	–	0.20	V
		I_O = 24 mA	3.0	–	–	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; note 2	3.6	–	±0.1	±5	μA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; V_O = 5.5 V or GND	3.6	–	0.1	±5	μA
I_{off}	power off leakage supply	V_I or V_O = 5.5 V	0.0	–	0.1	±10	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	3.6	–	0.1	20	μA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC}$–0.6V; I_O = 0	2.7 to 3.6	–	5	500	μA
I_{BHL}	bushold LOW sustaining current	V_I = 0.8 V; notes 3, 4 and 5	3.0	75	–	–	μA
I_{BHH}	bushold HIGH sustaining current	V_I = 2.0 V; notes 3, 4 and 5	3.0	–75	–	–	μA
I_{BHLO}	bushold LOW overdrive current	notes 3, 4 and 6	3.6	500	–	–	μA
I_{BHHO}	bushold HIGH overdrive current	notes 3, 4 and 6	3.6	–500	–	–	μA

Notes

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. For bushold parts, the bushold circuit is switched off when $V_I > V_{CC}$ allowing 5.5 V on the input terminal.
3. Valid for data inputs of bushold parts (74LVCH16244A) only.
4. For data inputs only, control inputs do not have a bushold circuit.
5. The specified sustaining current at the data input holds the input below the specified V_I level.
6. The specified overdrive current at the data input forces the data input to the opposite input state.

AC CHARACTERISTICS

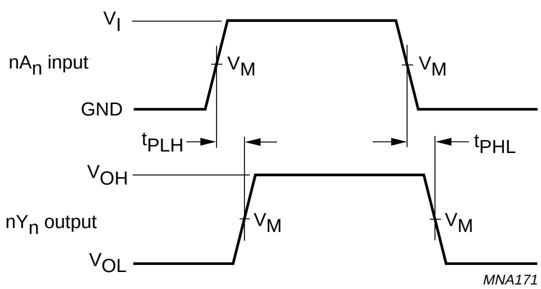
GND = 0 V; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = –40 to +85 °C							
t_{PHL}/t_{PLH}	propagation delay nA_n to nY_n	see Figs 6 and 8	1.2	–	11.0	–	ns
			2.7	1.5	–	5.5	ns
			3.0 to 3.6	1.5	3.0(1)	4.5	ns
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nY_n	see Figs 7 and 8	1.2	–	15.0	–	ns
			2.7	1.5	–	6.5	ns
			3.0 to 3.6	1.5	3.5(1)	5.5	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY_n	see Figs 7 and 8	1.2	–	10.0	–	ns
			2.7	1.5	–	6.2	ns
			3.0 to 3.6	1.5	3.7(1)	5.2	ns

Note

1. Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

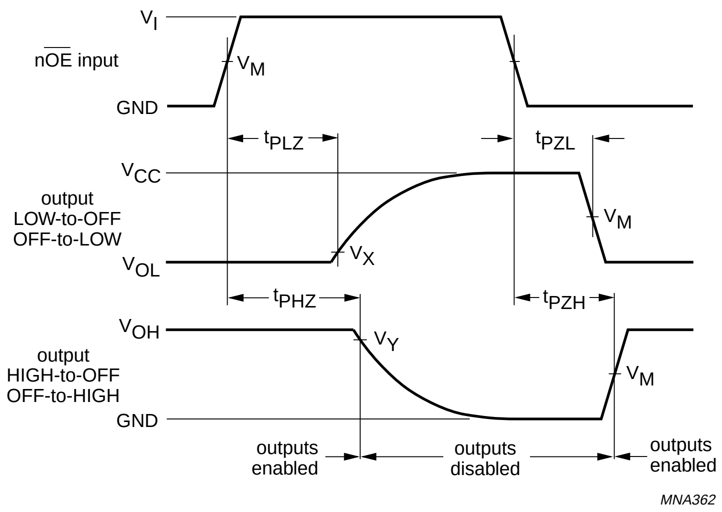
AC WAVEFORMS



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.2 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 The input nA_n to output nY_n propagation delays.

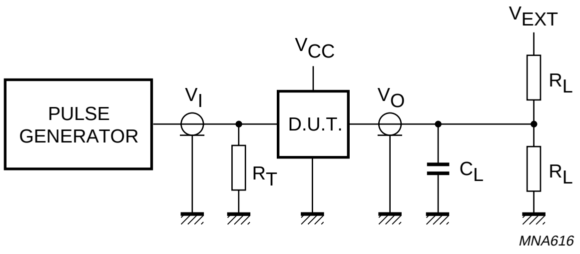


V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.2 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V;
$V_X = V_{OL} + 0.1$ V at $V_{CC} < 2.7$ V;
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V;
$V_Y = V_{OH} - 0.1$ V at $V_{CC} < 2.7$ V.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 3-state enable and disable times.



V_{CC}	V_I	C_L	R_L	V_{EXT}		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.2 V	V_{CC}	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

Definitions for test circuits:

R_L = Load resistor.

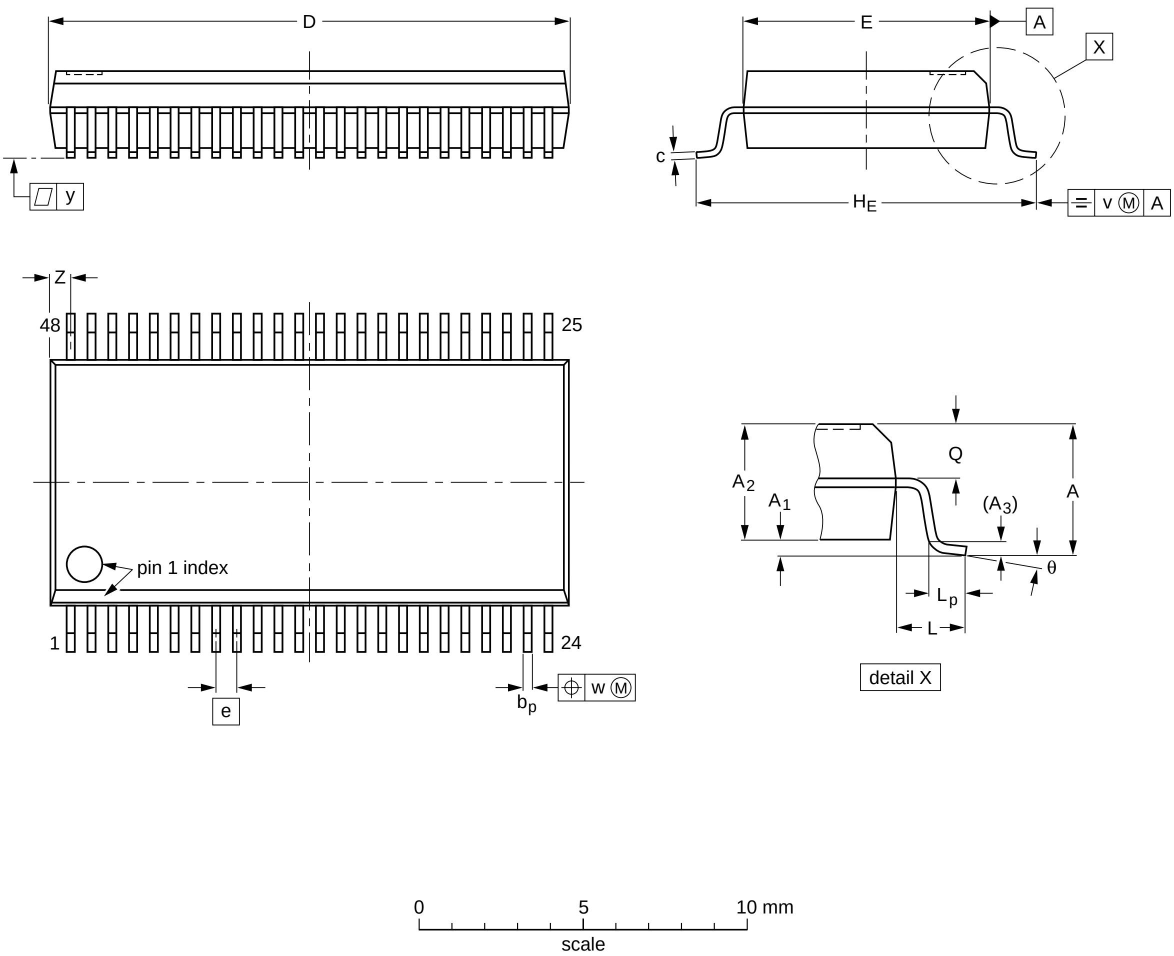
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.8 Load circuitry for switching times.

PACKAGE OUTLINES

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**

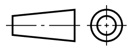


DIMENSIONS (mm are the original dimensions)

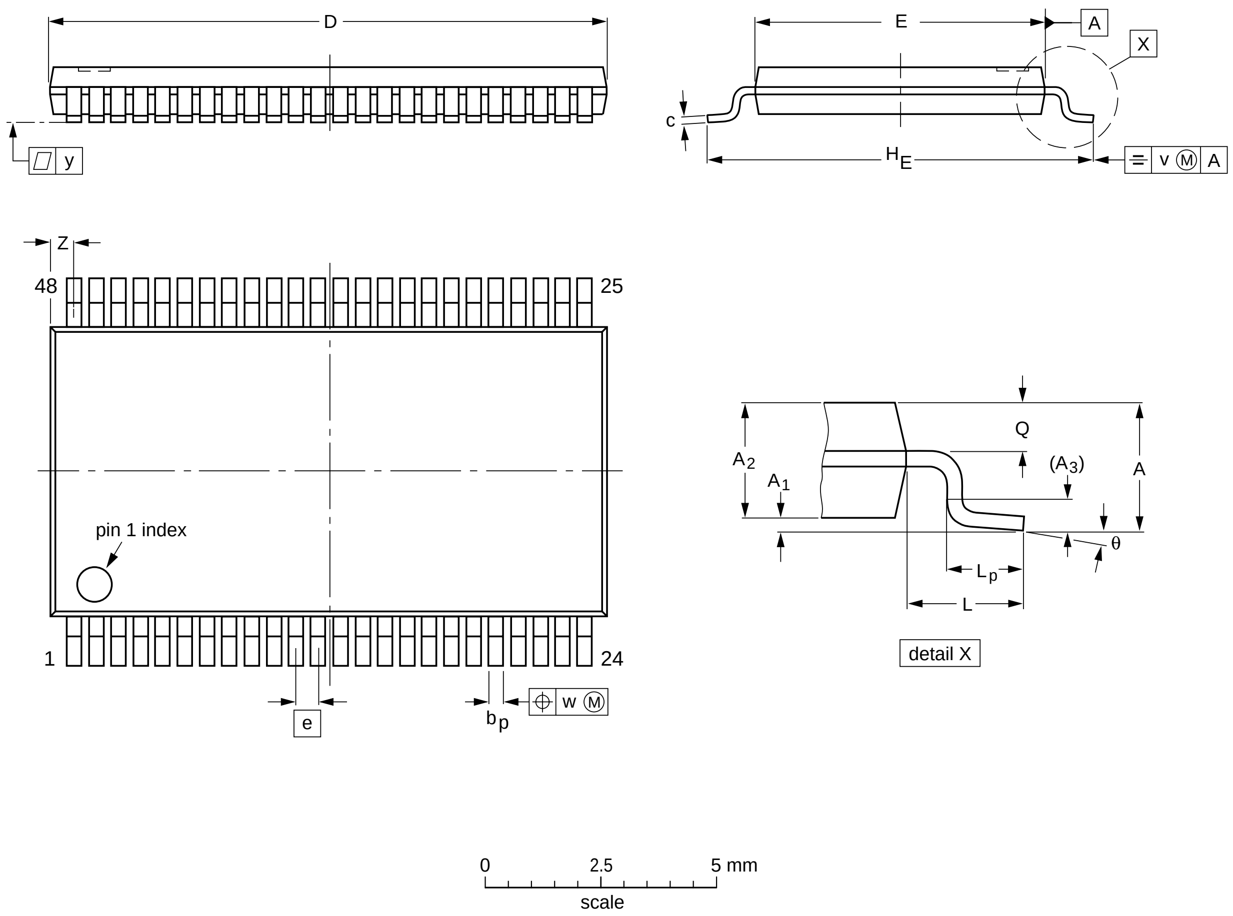
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118				~~95-02-04~~ 99-12-27

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

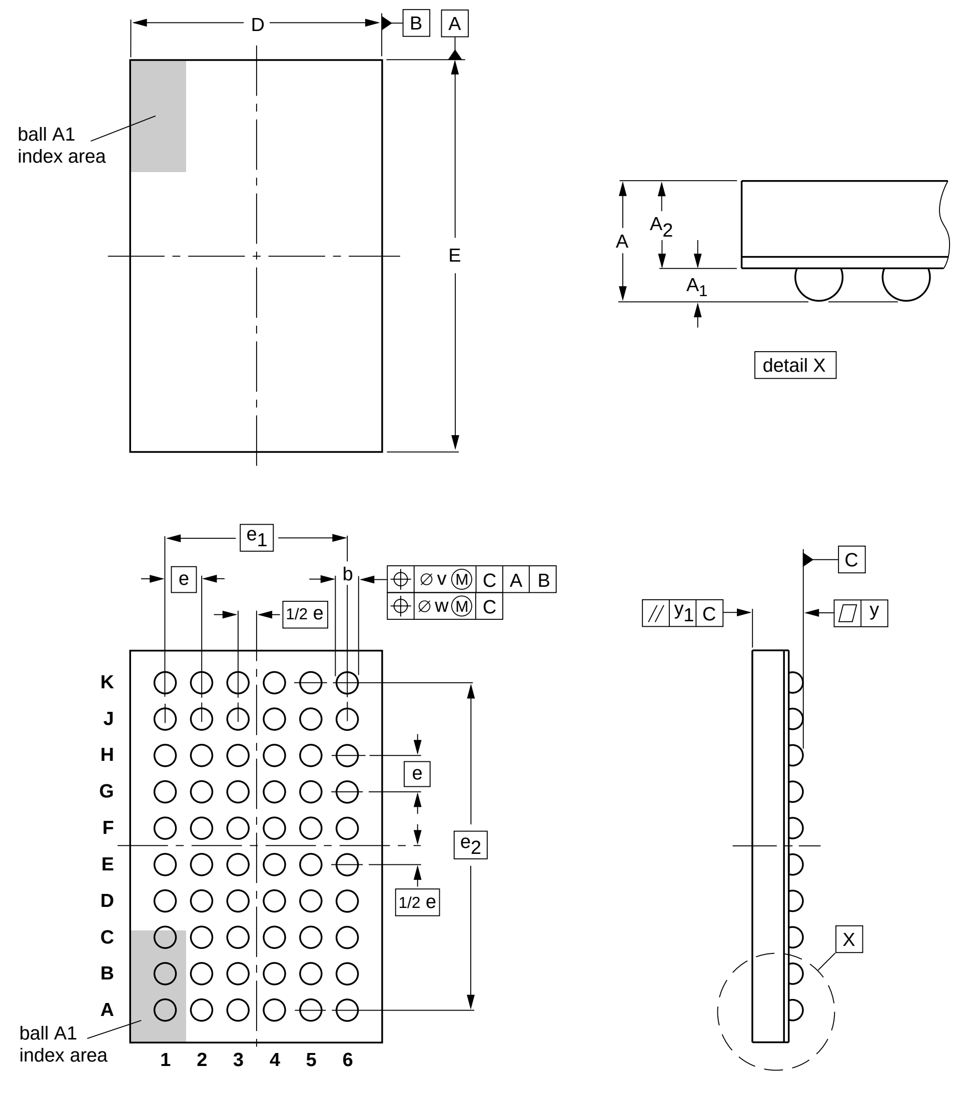
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

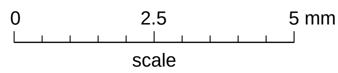
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT362-1		MO-153				~~95-02-10~~ 99-12-27

VFBGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 x 7 x 0.65 mm **SOT702-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1	0.3 0.2	0.7 0.6	0.45 0.35	4.6 4.4	7.1 6.9	0.65	3.25	5.85	0.15	0.08	0.08	0.1



OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT702-1		MO-225				~~01-06-25~~ 02-08-08

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *“(LF)BGA Application Note*” (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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NOTES

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